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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,061	12/15/2003	Christopher Olsen	AMAT/8629/FEP/GCM/RKK	4253

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EXAMINER	
SELLMAN, CACHET I	
ART UNIT	**PAPER NUMBER**
1762	

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,061	OLSEN ET AL.	
	Examiner	Art Unit	
	Cachet I. Sellman	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement is made of the amendment filed by the applicant on 5/11/2006, in which claims 1, 10, 13 and 15 were amended and claims 19-26 were cancelled. Claims 1-18 are currently pending in U.S. Application Serial No. 10\736,061.

Response to Arguments

1. Applicant's arguments filed 5/11/2006 have been fully considered but they are not persuasive. Applicant's arguments regarding the 35 USC 102(e) rejection of claims 1-3, 5, and 7-9 by Cheng et al. state that the "Cheng et al. reference does not teach or suggest forming a gate dielectric by providing a structure comprising a silicon oxide film forming on a substrate, heating the structure to incorporate nitrogen into the top surface of the silicon dioxide film, and then exposing the structure to a plasma comprising a nitrogen source to form a silicon oxynitride gate dielectric." However as stated in the previous office action, Cheng et al. does teach a process of forming a silicon oxide film on a silicon substrate, annealing (heating) the substrate in NH_3 which would inherently incorporate nitrogen into a top surface of the silicon oxide film, and then exposing the substrate to a plasma comprising a nitrogen source to form silicon oxynitride gate dielectric on the substrate. The applicant argues that although Cheng et al. teaches the use of NH_3 that Cheng et al. also teaches negative results when using the NH_3 therefore Cheng does not teach, suggest or motivate using NH_3. In the Cheng et al., reference it clearly states that NH_3, NO, or N_2 can be used meaning that the Cheng reference does teach the use of NH_3 as a source for the nitriding annealing process and therefore it anticipates the use of NH_3 in the process by one having ordinary skill in the art if the

product formed is not affected by electron trapping therefore Cheng et al. meets the limitations of claim 1 and the rejection is maintained.

2. Applicant's arguments regarding the rejection of claims 10-12, 14 and 16 states that the Cheng et al. and Kiryu et al. references does not suggest or motivate one to heat a structure comprising a silicon oxide film formed on a silicon substrate in an atmosphere comprising NH_3 in a processing chamber then transferring the structure to another processing chamber to expose the substrate to a plasma. However, using the process as described by Cheng et al. in the previous office action it would have been obvious to one having ordinary skill to modify the processing system of Kiryu et al. to include using different chambers for each step of the process to avoid contamination of the substrate as stated in the previous office action therefore the rejection of claims 10-12,14 and 16 is maintained.

3. Applicant's arguments regarding the rejection of claims 4 and 17 under 35 USC 103(a) over Cheng et al. in view of Kiryu et al. and in view of Nimi et al. states that Cheng et al., Kiryu et al. and Nimi et al. do not teach all of the limitations of independent claims 1 and 10, however as stated above in paragraphs 1 and 2 Cheng et al. and Kiryu et al. teach the limitations of the claims therefore the applicants arguments are not persuasive and the rejection is maintained.

4. Applicant's arguments regarding the rejection of claim 6 and 18 under 35 USC 103(a) over Cheng et al. in view of Kiryu and in further view of Ibok state that since none of the references (Cheng et al., Kiryu and Ibok) teach the limitations of independent claims 1 and 10 that the rejection should be traversed. However, for the

reasons stated above in paragraphs 1 and 2, Cheng et al. teaches the limitations of claim 1 and Cheng et al. in view of Kiryu teach the limitations of claim 10 therefore the applicant's arguments are not persuasive and the rejection is maintained.

5. Applicant's arguments regarding the rejection of claims 13 and 15 under 35 USC 103(a) over Cheng et al. in view of Kiryu et al. and further in view of Burnham states that the Burnham et al. does not teach the limitations of independent claims 1 and 10 that Cheng et al. and Kiryu lack therefore the rejection should be traversed. However, for the reasons stated above in paragraphs 1 and 2 the Cheng et al. reference does teach the limitations of claim 1 and the Cheng et al. in view of Kiryu references teach the limitations of claim 10 therefore the applicant's arguments are not considered persuasive and for that reason the rejection is maintained.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 5, and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (US 6649538).

Cheng et al. discloses a method for forming a nitrided gate oxide on a silicon substrate by first forming a silicon dioxide layer over the silicon substrate (abstract); followed by a nitriding annealing process in an ambient including NH_3 (column 4, lines 39-42); and then exposing the gate oxide to a plasma nitriding treatment comprising a nitrogen source (column 4, lines 56-63 and column 5, lines 7-10) as required by **claim 1**. The method includes the step of annealing the structure after exposing it to the plasma (column 6, lines 10 – 30) as required by **claim 2**. The annealing can be performed in an oxygen-containing atmosphere (column 6, lines 10-15, 19, and 22) as required by **claim 3.** The nitrogen source in the plasma nitriding treatment is N_2 (column 5, lines 7-8) as required by **claim 5**. The substrate is exposed to plasma at a pressure of 1milliTorr to about 50 milliTorr (column 5, lines 2-5) as required by **claim 7**. The silicon dioxide layer can be formed by oxidizing a top surface of the silicon substrate (column 4, lines 14-26) as required by **claim 8**. Heating the structure in a NH_3 atmosphere nitrites the structure without incorporating oxygen (column 4, lines 41-42) as required by **claims 9**.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10-12, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. as applied to claims 1-3, 5, and 7-9 stated above in view of Kiryu et al. (US 2004/0053472 A1).

The teachings of Cheng et al. as applied to claims 1-3, 5, and 7-9 are as stated above.

Cheng et al. does not teach using an integrated system to form the silicon oxynitride where the structure is heated in a NH_3 atmosphere in a first processing chamber then transferred to a second chamber where it is exposed to a plasma as required by **claim 10**.

Kiryu et al. discloses an apparatus for film formation of a gate insulator, which enables the formation of a gate of a high dielectric constant material using a cluster tool [0005]. The cluster tool performs various kinds of processes for an object such as film forming, annealing and removal of natural oxide film [0134]. The tool consists of processing chambers in which various processes can be performed a transfer chamber, load lock chamber, and a transfer arm that delivers the object to each processing chamber and once the film is formed the substrate is removed from the processing chamber. Using the cluster tool to form a gate insulator prevents contamination of the object by the atmosphere. When this apparatus is used for film formation of a gate insulator the process can be carried out successively with low burden [0143].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to perform the process taught by Cheng et al. in the apparatus of Kiryu et al. where a first processing chamber is used for heating the substrate in an NH_3 atmosphere; a second chamber is used for exposing the substrate to a plasma containing a nitrogen source. One would have been motivated to do so because Cheng et al. discloses a method for forming a high dielectric constant gate insulator (silicon oxynitride) and Kiryu et al. teaches that the apparatus can be used to form a high dielectric constant gate insulator such as silicon oxynitride using a substrate that has a layer of silicon dioxide [0014] where the insulator is not contaminated by the atmosphere and is formed with low burden and Kiryu et al. further states that the processing chambers of the apparatus can be used to perform the processes that are used by Cheng et al. to form the film (such as annealing and film forming) therefore one would have a reasonable expectation of success in forming the silicon oxynitride film without contamination of the film as well as with low burden.

Cheng et al. further teaches the step of annealing the substrate after exposing it to plasma (column 6, lines 10-30). Therefore it would have been obvious to transfer the substrate to a third processing chamber in order to perform the annealing step as required by **claim 11**. Cheng et al. discloses annealing the substrate in an atmosphere of O_2 (column 6, lines 10-15, 19, 22) as required by **claim 16**. Cheng et al. teaches that the silicon dioxide film is formed by oxidation (column 4, lines 14-26) and Kiryu et al. discloses that the processing chambers of the apparatus can be used for film forming

and that a silicon dioxide layer is formed first before the formation of the silicon oxynitride film [0014] therefore it would have been obvious to have a processing chamber for forming the silicon dioxide layer as required by **claims 12 and 14**.

10. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kiryu et al. as applied to claims 1 and 16 above in view of Niimi et al. (US 6548366 B2).

The teachings of Cheng et al. in view of Kiryu et al. as applied to claims 1 and 16 are as stated above.

Cheng et al. in view of Kiryu et al. does not teach annealing the structure in an inert or reducing atmosphere before annealing in an atmosphere comprising O_2 as required by **claims 4 and 17**.

Niimi et al. discloses a method of two-step annealing a silicon dioxide layer to form a uniform nitrogen profile within the layer. In the method disclosed a silicon dioxide layer is exposed to a nitrogen – containing plasma and reoxidized and annealed to stabilize the nitrogen distribution, heal plasma-induced damage and reduce interfacial defect density (abstract). The annealing and re-oxidation step consists of annealing the structure in a mixture of H_2 and N_2 gas then annealing it in a mixture of O_2 and N_2 gas to heal plasma-induced damage after nitrogen containing plasma exposure. Niimi et al.

further discloses that these two steps are executed consecutively without substantial delay between them (column 6, lines 14-35).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the process taught by Cheng et al. to include the step of annealing the structure in an inert atmosphere before annealing in an atmosphere of O_2. One would have been motivated to do so because both Cheng et al. and Niimi et al. disclose processes for forming an silicon oxynitride film that include using a silicon substrate with a silicon oxide film; exposing it to a plasma with a nitrogen source; and annealing in an oxygen atmosphere and Niimi et al. further discloses that by annealing in an inert atmosphere then in an atmosphere of O_2 heals plasma-induced damage as well as stabilize the nitrogen distribution in the film therefore one would have a reasonable expectation of success in forming the silicon oxynitride film with stabilized nitrogen distribution and that is healed from the damage induced by plasma.

11. Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kiryu as applied to claims 1 and 10 above, and further in view of Ibok (US 2001/0049186).

The teachings of Cheng et al. in view of Kiryu et al. as applied to claims 1 and 10 are stated above.

Cheng et al. in view of Kiryu et al. does not disclose heating the substrate in an atmosphere of NH_3 at a temperature of at least 700°C and at a pressure less than about 100 Torr as required by **claim 6** or placing the substrate in a cooling chamber after heating and before exposing it to a plasma as required by **claim 18**.

Ibok discloses a method for making a gate insulator on a silicon substrate, which includes the steps of forming a thin oxide film on the substrate then annealing the substrate in ammonia at a temperature up to 1100°C (abstract and [0017]).
It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the process of Cheng et al. in view of Kiryu et al. by heating the substrate at the temperatures disclosed by Ibok. One would have been motivated to do so because Cheng et al. in view of Kiryu et al. disclose a method for forming a gate insulator by heating a silicon substrate with a silicon oxide layer thereon in an atmosphere of NH3 to incorporate nitrogen in to the film but does not teach the annealing temperature and Ibok also teaches the same process with the goal of establishing a nitrogen concentration within the film [0017] therefore one would a reasonable expectation of success in forming the silicon oxynitride film.

The pressure limitation is not taught by Cheng et al. discloses that the plasma process occurs at a pressure of about 1 milliTorr to about 100 milliTorr (column 4, lines 61-63). One would have been motivated to heat the substrate at these pressures in

order to use the same processing chamber for two steps, which would result in less time to form the silicon oxynitride layer.

In regards to **claim 18**, where the applicant requires the use of a cool down chamber after heating and before transferring to a second processing chamber, It would have been obvious to one having ordinary skill in the art to include a cool down chamber when going from a heating step where the temperature can get up to 1100°C to a step where the substrate is being exposed to a plasma at a temperature of about 300 – 400°C (Cheng et al. column 4, lines 64 - column 5, lines 1-5).

12. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kiryu et al. as applied to claims 1 and 10 above, and further in view of Burnham et al. (US 6649538 B1).

The teachings of Cheng et al. in view of Kiryu et al. as applied to claims 1 and 10 are as stated above.

Cheng et al. in view of Kiryu et al. does not disclose forming a polysilicon layer on the substrate as required by claims **13 and 15**.

Burnham et al. discloses a method for forming a MOSFET transistor, which includes a silicon substrate, and a polysilicon gate formed on top of a thin gate dielectric layer where the thin gate dielectric layer is silicon oxynitride (column 1, lines 17-25).

It would have been obvious to one having ordinary skill at the time the invention was made to modify the process taught by Cheng et al. in view of Kiryu et al. to include the step of forming a polysilicon gate layer on top of the silicon oxynitride. One would have been motivated to do so because Cheng et al. discloses that this process of forming a silicon oxynitride film can be used for a MOSFET where a gate electrode is formed over a gate dielectric and Burnham et al. teaches that the polysilicon (gate electrode) can be formed over a thin gate dielectric layer (silicon oxynitride) therefore one would have a reasonable expectation of success in forming the MOSFET.

In regards to **claim 15**, where the applicant requires that the substrate is transferred to a fifth processing chamber that is external to the integrated processing system where the polysilicon layer is deposited, it would have been obvious to one having ordinary skill in the art that to transfer the substrate to another processing chamber because Kiryu et al. discloses that the substrate can be removed from the process after the formation of the gate electrode (silicon oxynitride).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cachet I. Sellman whose telephone number is 571-272-0691. The examiner can normally be reached on Monday through Friday, 7:00 - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cachet I Sellman
Examiner
Art Unit 1762

TIMOTHY MEEKS
SUPERVISORY PATENT EXAMINER